The 74xxx Databook

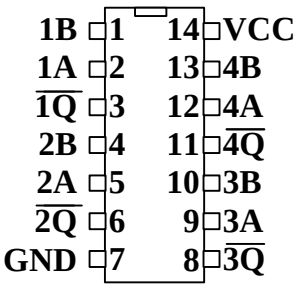
There is the pinlayout, the connectionlayout, an functiontable and the most important specifications available for every IC (74...,74H...,74L...,74LS... and 74S...).
The databook is still in work, but you can already now start to use it. I keep updating it on an continious base.You can always download the most current version at “http://home.t-online.de/home/G-Bauer/datash.htm“.
If you find any mistakes please let me know and write an email to ”andre-bauer@gmx.de”

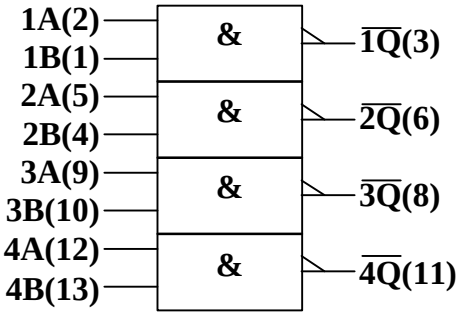
Das 74xxx Datenbuch

Für jedes IC ist die Pinbelegung, ein Anschlußschema sowie eine Funktionstabelle vorhanden. Zudem sind unter anderem die Stromaufnahme, der Ausgangsstrom und die Geschwindigkeit jeweils für 74...,74H...,74L...,74LS... und 74S... angegeben.
Das Datenbuch ist noch in Arbeit, aber man kann es schon benutzen und sobald ich es weiter geschrieben habe kannst Du es hier downloaden: “http://home.t-online.de/home/G-Bauer/datash2.htm“
Wenn du darin Fehler findest (nobody is perfect) schicke bitte ein email an ”andre-bauer@gmx.de”

74x00:

Quad 2 input NAND gate
Vier NAND Gatter mit je 2 Eingängen



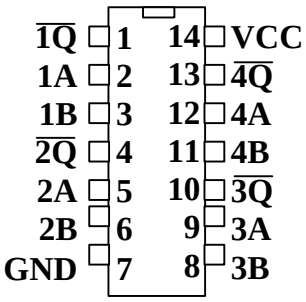


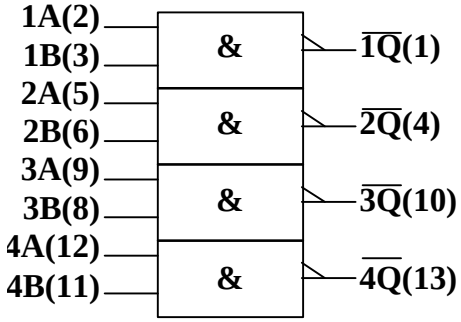
INPUT		OUTPUT
A	B	$\overline{Q}$
H	H	L
X	L	H
L	X	H

Some recommended conditions	7400	74H00	74L00	74LS00	74S00	UNIT
Supply current with all outputs high	8	16,8	0,8	1,6	16	mA
Supply current with all outputs low	22	40	2,04	4,4	36	mA
High-level input current	40	50	10	20	50	µA
Low-level input current	-1,6	-2	-0,18	-0,4	-2	mA
High-level output current	-400	-500	-200	-400	-1000	µA
Low-level output current	16	20	3,6	8	20	mA
Output max delay, low to high level	22	10	60	15	4,5	ns
Output max delay, high to low level	15	10	60	15	5	ns

74x01:

Quad 2 input NAND gate, open-drain outputs
Vier NAND Gatter mit je 2 Eingängen, open-drain Ausgänge



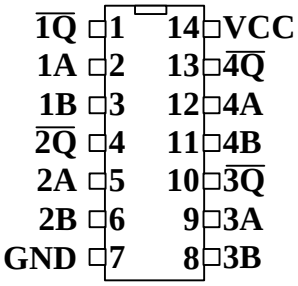


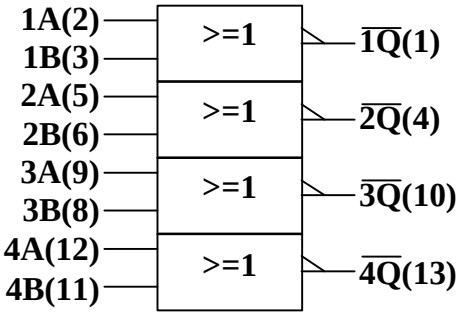
INPUT		OUTPUT
A	B	$\overline{Q}$
H	H	L
X	L	H
L	X	H

Some recommended conditions	7401	74H01	74L01	74LS01	74S01	UNIT
Supply current with all outputs high	8	10	0,8	1,6	13,2	mA
Supply current with all outputs low	22	40	2,04	4,4	36	mA
High-level input current	40	50	10	20	50	µA
Low-level input current	-1,6	-2	-0,18	-0,4	-2	mA
High-level output current	250	250	50	100	250	µA
Low-level output current	16	20	3,6	8	20	mA
Output max delay, low to high level	45	15	90	32	7,5	ns
Output max delay, high to low level	15	12	60	28	7	ns

74x02:

Quad 2 input NOR gate
Vier NOR Gatter mit je 2 Eingängen



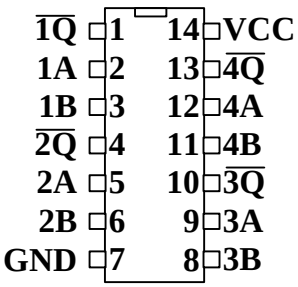


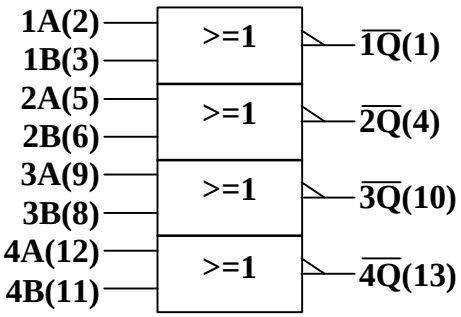
INPUT		OUTPUT
A	**B**	$\overline{\mathbf{Q}}$
H	X	L
X	H	L
L	L	H

Some recommended conditions	7402	74H02	74L02	74LS02	74S02	UNIT
Supply current with all outputs high	16		1,6	3,2	29	mA
Supply current with all outputs low	27		2,6	5,4	45	mA
High-level input current	40		10	20	50	µA
Low-level input current	-1,6		-0,18	-0,4	-2	mA
High-level output current	-400		-200	-400	-1000	µA
Low-level output current	16		3,6	8	20	mA
Output max delay, low to high level	15		60	15	5,5	ns
Output max delay, high to low level	15		60	15	5,5	ns

74x03:

Quad 2 input NOR gate, open-drain outputs
Vier NOR Gatter mit je 2 Eingängen, open-drain Ausgänge



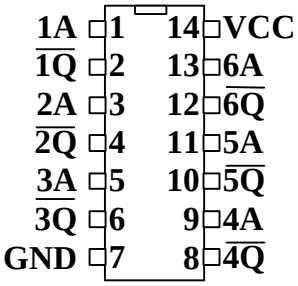


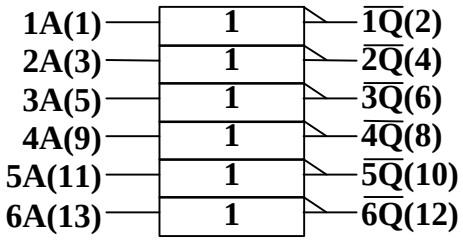
INPUT		OUTPUT
A	**B**	$\overline{\mathbf{Q}}$
H	X	L
X	H	L
L	L	H

Some recommended conditions	7403	74H03	74L03	74LS03	74S03	UNIT
Supply current with all outputs high	8		0,8	1,6	13,2	mA
Supply current with all outputs low	22		2,04	4,4	36	mA
High-level input current	40		10	20	50	µA
Low-level input current	-1,6		-0,18	-0,4	-2	mA
High-level output current	250		50	100	250	µA
Low-level output current	16		3,6	8	20	mA
Output max delay, low to high level	45		90	32	7,5	ns
Output max delay, high to low level	15		60	28	7,5	ns

74X04:

Hex INVERTER
Sechs INVERTER



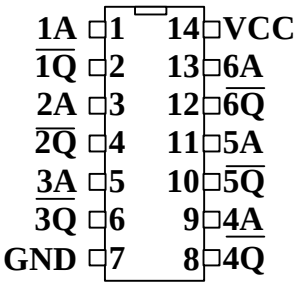


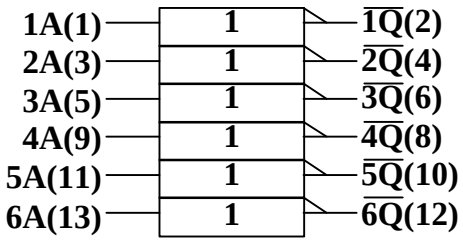
INPUT	OUTPUT
A	$\overline{Q}$
L	H
H	L

Some recommended conditions	7404	74H04	74L04	74LS04	74S04	UNIT
Supply current with all outputs high	12	26	1,2	2,4	24	mA
Supply current with all outputs low	33	58	3,06	6,6	54	mA
High-level input current	40	50	10	20	50	µA
Low-level input current	-1,6	-2	-0,18	-0,4	-2	mA
High-level output current	-400	-500	-200	-400	-1000	µA
Low-level output current	16	20	3,6	8	20	mA
Output max delay, low to high level	22	10	60	15	4,5	ns
Output max delay, high to low level	15	10	60	15	5	ns

74X05:

Hex INVERTER, open-drain outputs
Sechs INVERTER, open-drain Ausgängen



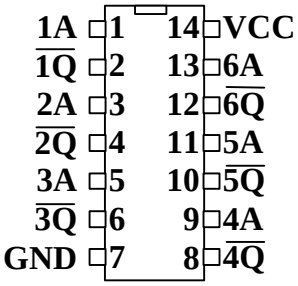


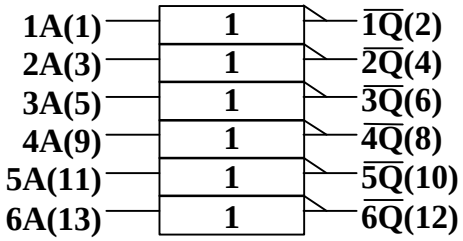
INPUT	OUTPUT
A	$\overline{Q}$
L	H
H	L

Some recommended conditions	7405	74H05	74L05	74LS05	74S05	UNIT
Supply current with all outputs high	12	26		2,4	19,8	mA
Supply current with all outputs low	33	58		6,6	54	mA
High-level input current	40	50		20	50	µA
Low-level input current	-1,6	-2		-0,4	-2	mA
High-level output current	250	250		100	250	µA
Low-level output current	16	20		8	20	mA
Output max delay, low to high level	55	15		32	7,5	ns
Output max delay, high to low level	15	12		28	7	ns

74x06:

Hex DRIVER, inverting, open-drain outputs (30V)
Sechs Treiber, invertierend, open-drain Ausgänge (30V)



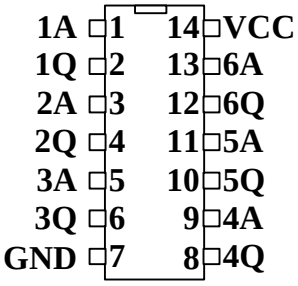


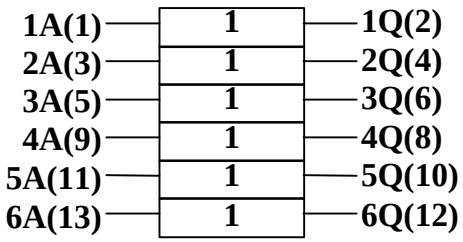
INPUT	OUTPUT
A	Q
L	H
H	L

Some recommended conditions	7406	74H06	74L06	74LS06	74S06	UNIT
Supply current with all outputs high	46					mA
Supply current with all outputs low	51					mA
High-level input current	40					µA
Low-level input current	-1,6					mA
High-level output current						µA
Low-level output current	40					mA
Output max delay, low to high level	15					ns
Output max delay, high to low level	23					ns

74x07:

HEX DRIVER, non inverting, open drain outputs(30V)
Sechs Treiber, nicht invertierend, open-drain Ausgänge (30V)



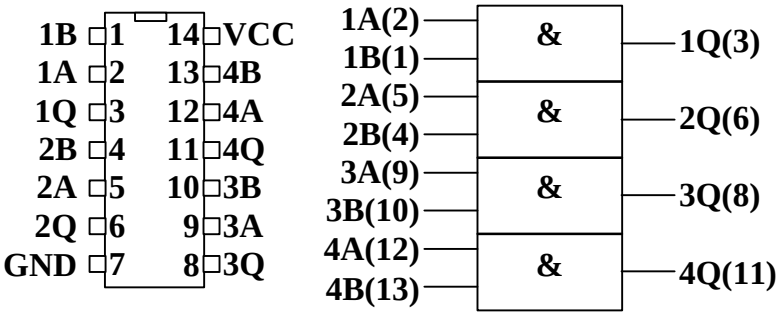


INPUT	OUTPUT
A	Q
H	H
L	L

Some recommended conditions	7407	74H07	74L07	74LS07	74S07	UNIT
Supply current with all outputs high	46					mA
Supply current with all outputs low	51					mA
High-level input current	40					µA
Low-level input current	-1,6					mA
High-level output current						µA
Low-level output current	40					mA
Output max delay, low to high level	15					ns
Output max delay, high to low level	23					ns

74x08:

Quad 2 input AND gate
Vier AND Gatter mit je 2 Eingängen

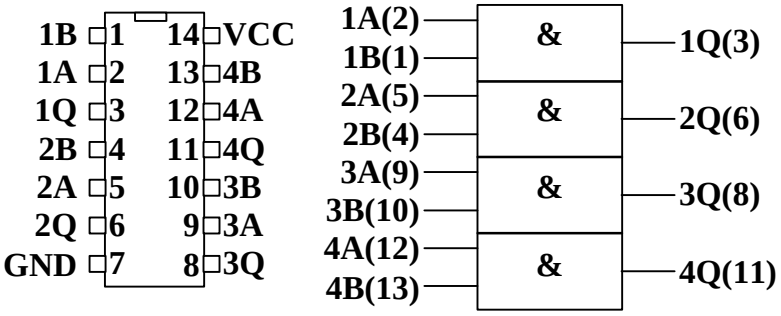


INPUT		OUTPUT
A	B	Q
H	H	H
X	L	L
L	X	L

Some recommended conditions	7408	74H08	74L08	74LS08	74S08	UNIT
Supply current with all outputs high	21	30		4,8	32	mA
Supply current with all outputs low	33	48		8,8	57	mA
High-level input current	40	50		20	50	µA
Low-level input current	-1,6	-2		-0,4	-2	mA
High-level output current	-800	-500		-400	-1000	µA
Low-level output current	16	20		8	20	mA
Output max delay, low to high level	27	12		15	7	ns
Output max delay, high to low level	19	12		20	7,5	ns

74x09:

Quad 2 input NAND gate, open-drain outputs
Vier NAND Gatter mit je 2 Eingängen, open-drain Ausgänge

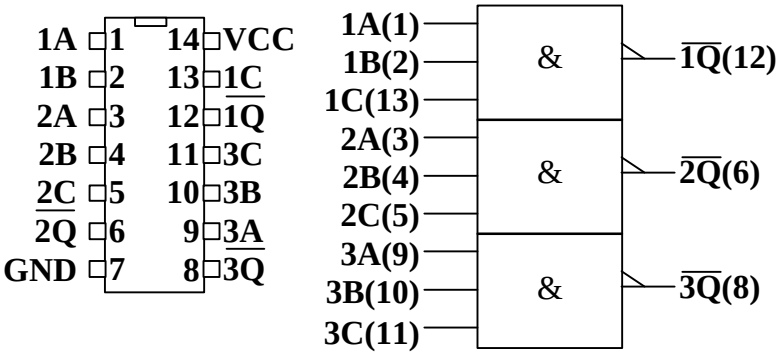


INPUT		OUTPUT
A	B	Q
H	H	H
X	L	L
L	X	L

Some recommended conditions	7409	74H09	74L09	74LS09	74S09	UNIT
Supply current with all outputs high	21	25		4,8	32	mA
Supply current with all outputs low	33	48		8,8	57	mA
High-level input current	40	50		20	50	µA
Low-level input current	-1,6	-2		-0,4	-2	mA
High-level output current						µA
Low-level output current	16	20		8	20	mA
Output max delay, low to high level	32	18		35	10	ns
Output max delay, high to low level	24	13		35	10	ns

74x10:

Triple 3 input NAND gate
Drei NAND Gatter mit je 3 Eingängen

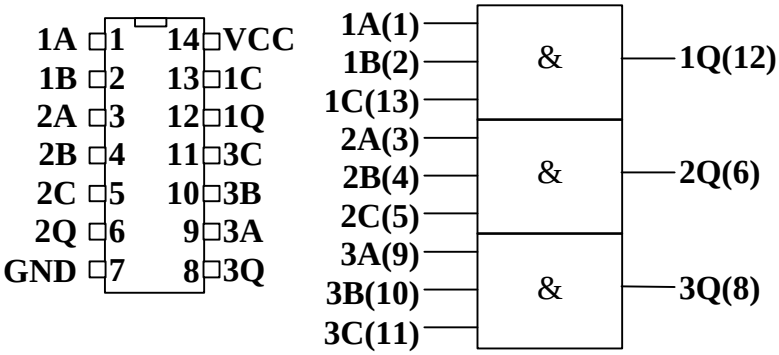


INPUT			OUTPUT
A	**B**	**C**	**$\overline{Q}$**
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

Some recommended conditions	7410	74H10	74L10	74LS10	74S10	UNIT
Supply current with all outputs high	6	12,6	0,6	1,2	12	mA
Supply current with all outputs low	16,5	30	1,53	3,3	27	mA
High-level input current	40	50	10	20	50	µA
Low-level input current	-1,6	-2	-0,18	-0,4	-2	mA
High-level output current	-400	-500	-200	-400	-1000	µA
Low-level output current	16	20	3,6	8	20	mA
Output max delay, low to high level	22	10	60	15	4,5	ns
Output max delay, high to low level	15	10	60	15	5	ns

74x11:

Triple 3 input AND gate
Drei AND Gatter mit je 3 Eingängen

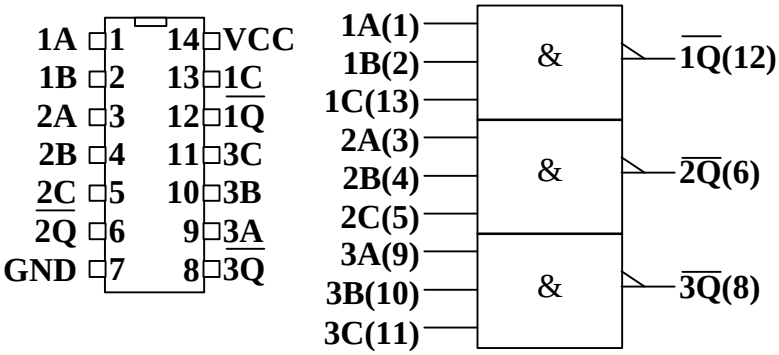


INPUT			OUTPUT
A	**B**	**C**	**Q**
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

Some recommended conditions	7411	74H11	74L11	74LS11	74S11	UNIT
Supply current with all outputs high		30		3,6	24	mA
Supply current with all outputs low		48		6,6	42	mA
High-level input current		50		20	50	µA
Low-level input current		-2		-0,4	-2	mA
High-level output current		-500		-400	-1000	µA
Low-level output current		20		8	20	mA
Output max delay, low to high level		12		15	7	ns
Output max delay, high to low level		12		20	7,5	ns

74x12:

Triple 3 input NAND gate, open-drain outputs
Drei NAND Gatter mit je 3 Eingängen, open-drain Ausgänge

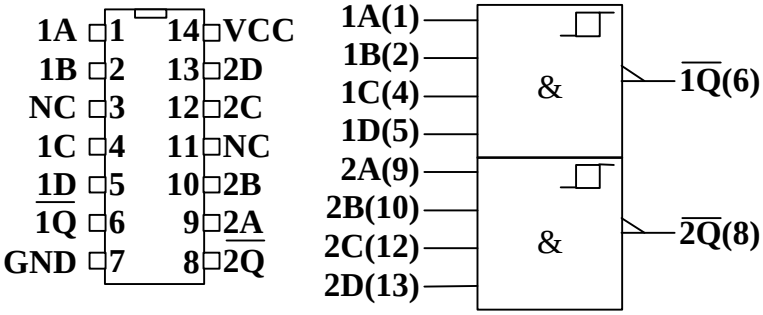


INPUT			OUTPUT
A	**B**	**C**	$\overline{\mathbf{Q}}$
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

Some recommended conditions	7412	74H12	74L12	74LS12	74S12	UNIT
Supply current with all outputs high	6			1,4		mA
Supply current with all outputs low	16,5			3,3		mA
High-level input current	40			20		µA
Low-level input current	-1,6			-0,4		mA
High-level output current	250			100		µA
Low-level output current	16			8		mA
Output max delay, low to high level	45			32		ns
Output max delay, high to low level	15			28		ns

74x13:

Dual 4 input NAND gate, schmitt-trigger inputs
Zwei NAND Gatter mit je 4 schmitt-trigger Eingängen

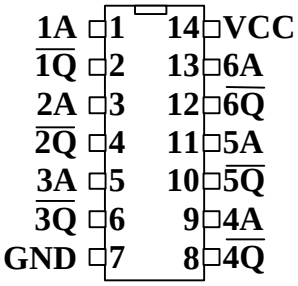


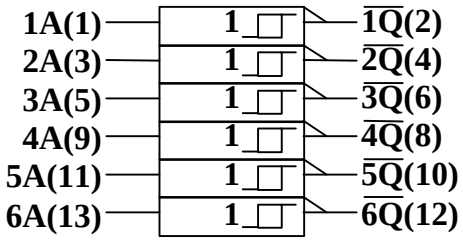
INPUT				OUTPUT
A	**B**	**C**	**D**	**Q**
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

Some recommended conditions	7413	74H13	74L13	74LS13	74S13	UNIT
Supply current with all outputs high	23			6		mA
Supply current with all outputs low	32			7		mA
High-level input current	40			20		µA
Low-level input current	-1,6			-0,4		mA
High-level output current	-800			-400		µA
Low-level output current	16			8		mA
Output max delay, low to high level	27			22		ns
Output max delay, high to low level	22			27		ns

74x14:

Hex INVERTER, schmitt-trigger inputs
Sechs INVERTER, schmitt-trigger Eingänge



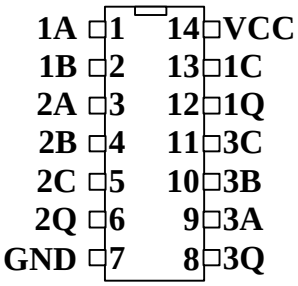


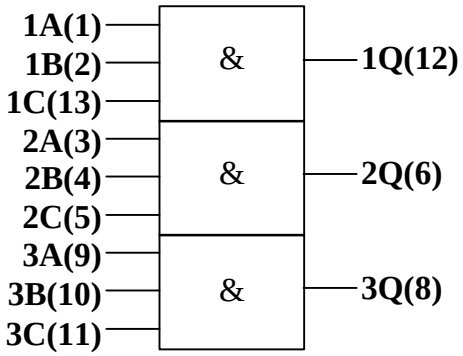
INPUT	OUTPUT
A	Q
L	H
H	L

Some recommended conditions	7414	74H14	74L14	74LS14	74S14	UNIT
Supply current with all outputs high	36			16		mA
Supply current with all outputs low	60			21		mA
High-level input current	40			20		µA
Low-level input current	-1,6			-0,4		mA
High-level output current	-800			-400		µA
Low-level output current	16			8		mA
Output max delay, low to high level	22			22		ns
Output max delay, high to low level	22			22		ns

74x15:

Triple 3 input AND gate, open-drain outputs
Drei AND Gatter mit je 3 Eingängen, open-drain Ausgänge



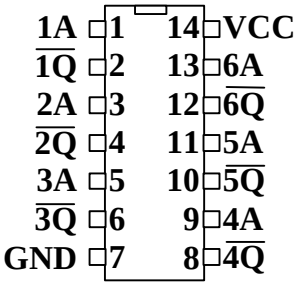


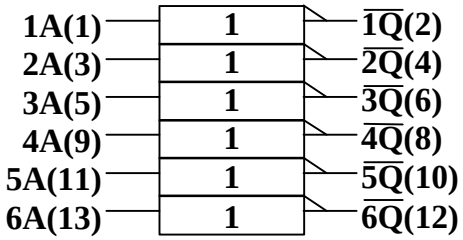
INPUT			OUTPUT
A	B	C	Q
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

Some recommended conditions	7415	74H15	74L15	74LS15	74S15	UNIT
Supply current with all outputs high		25		3,6	19,5	mA
Supply current with all outputs low		48		6,6	42	mA
High-level input current		50		20	50	µA
Low-level input current		-2		-0,4	-2	mA
High-level output current		250		100	250	µA
Low-level output current		20		8	20	mA
Output max delay, low to high level		18		35	8,5	ns
Output max delay, high to low level		13		35	9	ns

74x16:

Hex DRIVER, inverting, open-drain outputs (15V)
Sechs Treiber, invertierend, open-drain Ausgänge (15V)



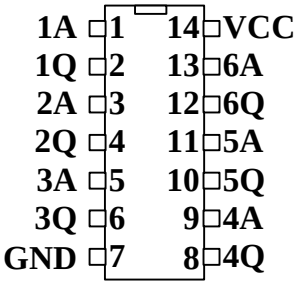


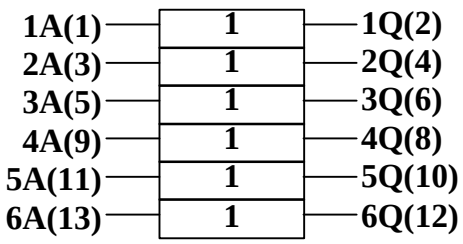
INPUT	OUTPUT
A	Q
L	H
H	L

Some recommended conditions	7416	74H16	74L16	74LS16	74S16	UNIT
Supply current with all outputs high	46					mA
Supply current with all outputs low	51					mA
High-level input current	40					µA
Low-level input current	-1,6					mA
High-level output current						µA
Low-level output current	40					mA
Output max delay, low to high level	15					ns
Output max delay, high to low level	23					ns

74x17:

HEX DRIVER, non inverting, open drain outputs(15V)
Sechs Treiber, nicht invertierend, open-drain Ausgänge (15V)



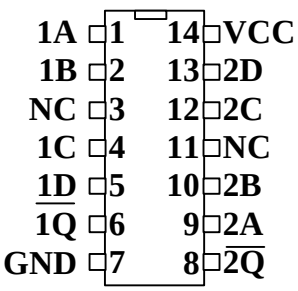


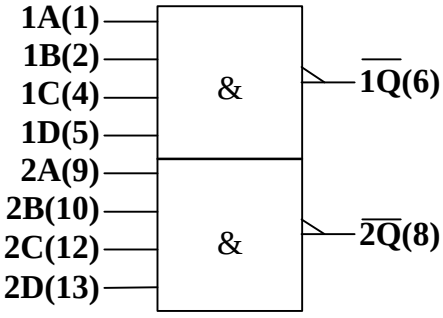
INPUT	OUTPUT
A	Q
H	H
L	L

Some recommended conditions	7417	74H17	74L17	74LS17	74S17	UNIT
Supply current with all outputs high	46					mA
Supply current with all outputs low	51					mA
High-level input current	40					µA
Low-level input current	-1,6					mA
High-level output current						µA
Low-level output current	40					mA
Output max delay, low to high level	15					ns
Output max delay, high to low level	23					ns

74x20:

Dual 4 input NAND gate
Zwei NAND Gatter mit je 4 Eingängen



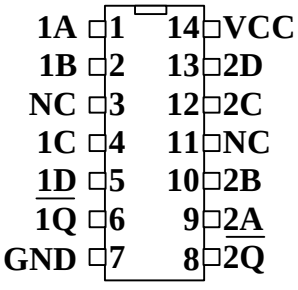


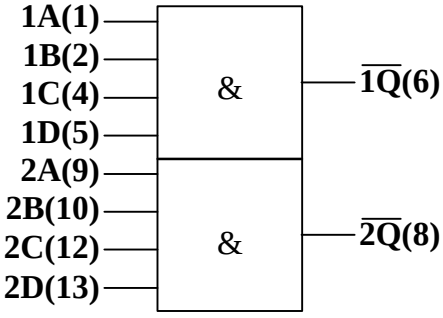
INPUT				OUTPUT
A	**B**	**C**	**D**	**$\overline{Q}$**
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

Some recommended conditions	7420	74H20	74L20	74LS20	74S20	UNIT
Supply current with all outputs high	4	8,4	0,4	0,8	8	mA
Supply current with all outputs low	11	20	1,02	2,2	18	mA
High-level input current	40	50	10	20	50	µA
Low-level input current	-1,6	-2	-0,18	-0,4	-2	mA
High-level output current	-400	-500	-200	-400	-1000	µA
Low-level output current	16	20	3,6	8	20	mA
Output max delay, low to high level	22	10	60	15	4,5	ns
Output max delay, high to low level	15	10	60	15	5	ns

74x21:

Dual 4 input AND gate
Zwei AND Gatter mit je 4 Eingängen



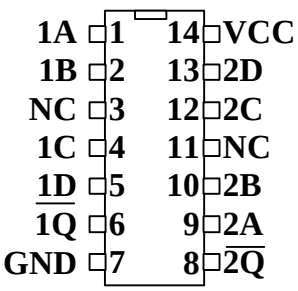


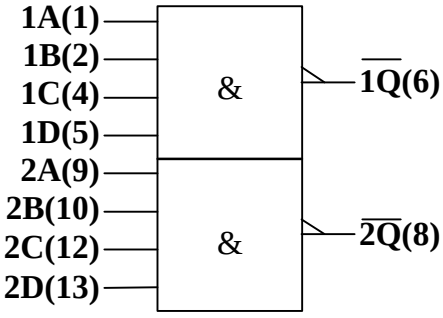
INPUT				OUTPUT
A	**B**	**C**	**D**	**$\overline{Q}$**
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

Some recommended conditions	7421	74H21	74L21	74LS21	74S21	UNIT
Supply current with all outputs high		20		2,4		mA
Supply current with all outputs low		32		4,4		mA
High-level input current		50		20		µA
Low-level input current		-2		-0,4		mA
High-level output current		-500		-400		µA
Low-level output current		20		8		mA
Output max delay, low to high level		12		15		ns
Output max delay, high to low level		12		20		ns

74x22:

Dual 4 input NAND gate, open drain outputs
Zwei NAND Gatter mit je 4 Eingängen, open-drain Ausgänge



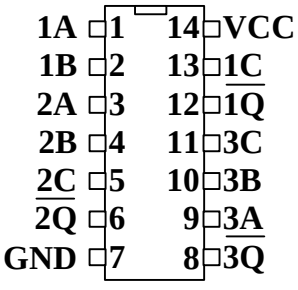


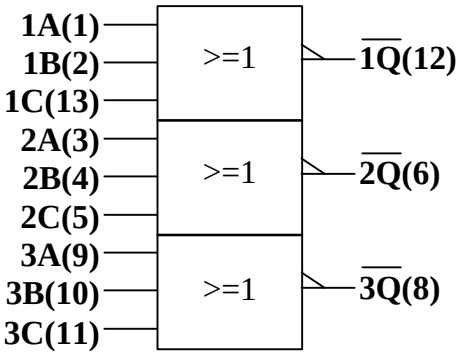
INPUT				OUTPUT
A	**B**	**C**	**D**	$\overline{\mathbf{Q}}$
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

Some recommended conditions	7422	74H22	74L22	74LS22	74S22	UNIT
Supply current with all outputs high	4	5		0,8	6,6	mA
Supply current with all outputs low	11	20		2,2	18	mA
High-level input current	40	50		20	50	µA
Low-level input current	-1,6	-2		-0,4	-2	mA
High-level output current	250	250		100	250	µA
Low-level output current	16	20		8	20	mA
Output max delay, low to high level	45	15		32	7,5	ns
Output max delay, high to low level	15	12		28	7	ns

74x27:

Triple 3 input NOR gate
Drei NOR Gatter mit je 3 Eingängen



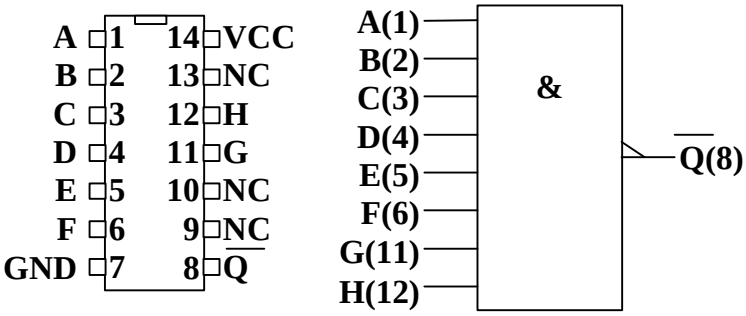


INPUT			OUTPUT
A	**B**	**C**	**Q**
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

Some recommended conditions	7427	74H27	74L27	74LS27	74S27	UNIT
Supply current with all outputs high	16			4		mA
Supply current with all outputs low	26			6,8		mA
High-level input current	40			20		µA
Low-level input current	-1,6			-0,4		mA
High-level output current	-400			-400		µA
Low-level output current	16			8		mA
Output max delay, low to high level	15			15		ns
Output max delay, high to low level	11			15		ns

74x30:

8 input NAND gate
NAND Gatter mit 8 Eingängen

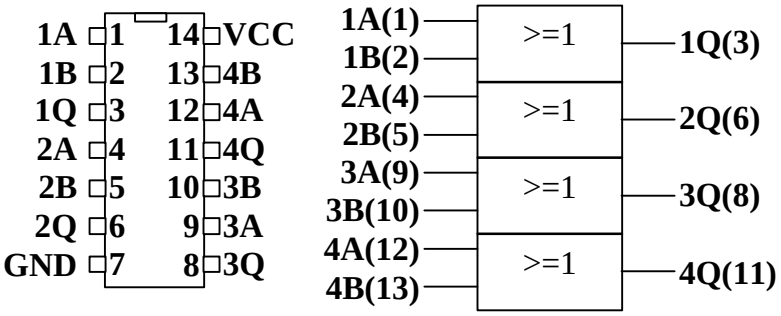


INPUT	OUTPUT
A-H	Q
all inputs H	L
one or more inputs L	H

Some recommended conditions	7430	74H30	74L30	74LS30	74S30	UNIT
Supply current with all outputs high	2	4,2	0,2	0,5	5	mA
Supply current with all outputs low	6	10	0,51	1,1	10	mA
High-level input current	40	50	10	20	50	µA
Low-level input current	-1,6	-2	-0,18	-0,4	-2	mA
High-level output current	-400	-500	-200	-400	-1000	µA
Low-level output current	16	20	3,6	8	20	mA
Output max delay, low to high level	22	10	60	15	6	ns
Output max delay, high to low level	15	12	100	20	7	ns

74x32:

Quad 2 input OR gate
Vier OR Gatter mit je 2 Eingängen

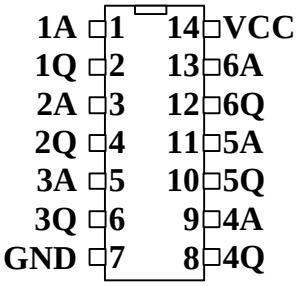


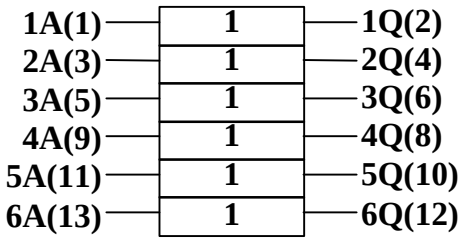
INPUT		OUTPUT
A	B	Q
H	X	H
X	H	H
L	L	L

Some recommended conditions	7432	74H32	74L32	74LS32	74S32	UNIT
Supply current with all outputs high	22			6,2	32	mA
Supply current with all outputs low	38			9,8	68	mA
High-level input current	40			20	50	µA
Low-level input current	-1,6			-0,4	-2	mA
High-level output current	-800			-400	-1000	µA
Low-level output current	16			8	20	mA
Output max delay, low to high level	15			22	7	ns
Output max delay, high to low level	22			22	7	ns

74x34:

Hex DRIVER, non inverting
Sechs Treiber, nicht invertierend



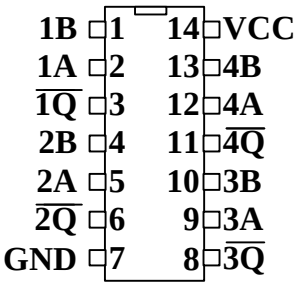


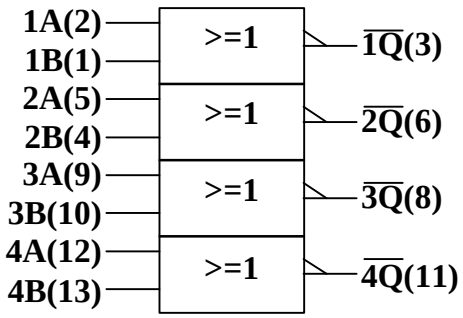
INPUT	OUTPUT
A	Q
H	H
L	L

Some recommended conditions	7434	74H34	74L34	74LS34	74S34	UNIT
Supply current with all outputs high						mA
Supply current with all outputs low						mA
High-level input current						µA
Low-level input current						mA
High-level output current						µA
Low-level output current						mA
Output max delay, low to high level						ns
Output max delay, high to low level						ns

74x36:

Quad 2 input NOR gate
Vier NOR Gatter mit je 2 Eingängen



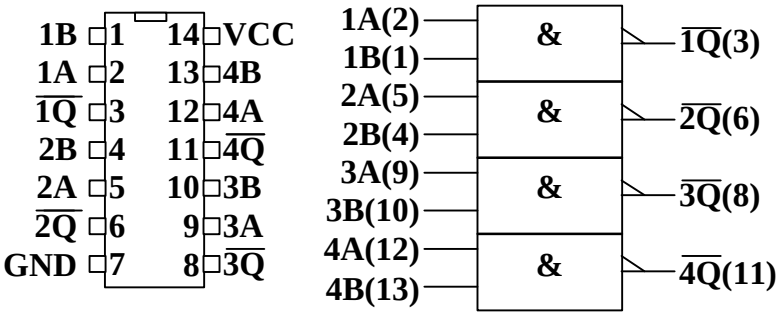


INPUT		OUTPUT
A	B	Q
H	X	L
X	H	L
L	L	H

Some recommended conditions	7436	74H36	74L36	74LS36	74S36	UNIT
Supply current with all outputs high						mA
Supply current with all outputs low						mA
High-level input current						µA
Low-level input current						mA
High-level output current						µA
Low-level output current						mA
Output max delay, low to high level						ns
Output max delay, high to low level						ns

74x38:

Quad 2 input NAND power-gate, FQ=30, open drain outputs
Vier NAND Leistungs-Gatter mit je zwei Engängen, FQ=30, open drain Ausgänge

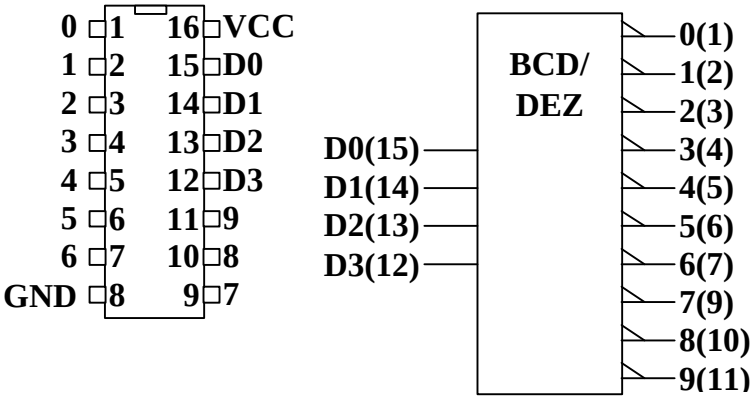


INPUT		OUTPUT
A	B	$\overline{Q}$
H	H	L
X	L	H
L	X	H

Some recommended conditions	7438	74H38	74L38	74LS38	74S38	UNIT
Supply current with all outputs high				2	36	mA
Supply current with all outputs low				12	80	mA
High-level input current				20	100	µA
Low-level input current				-0,4	-4	mA
High-level output current				250	250	µA
Low-level output current				24	60	mA
Output max delay, low to high level				32	10	ns
Output max delay, high to low level				28	10	ns

74x42:

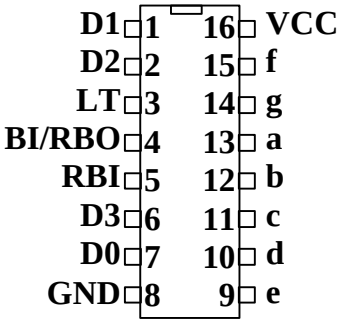
BCD to decimal decoder
BCD zu dezimal Dekoder

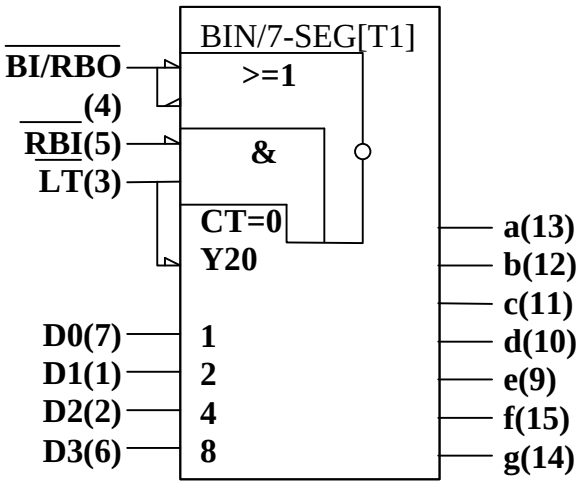


INPUT				OUTPUT
D3	D2	D1	D0	Q=L
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	-
H	L	H	H	-
H	H	L	L	-
H	H	L	H	-
H	H	H	L	-
H	H	H	H	-

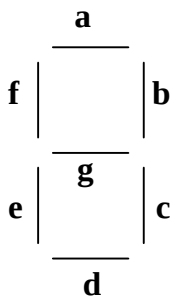
74x48:

BCD to 7 segment decoder/driver (5,5V)
BCD zu 7 Segment Dekoder/Treiber (5,5V)





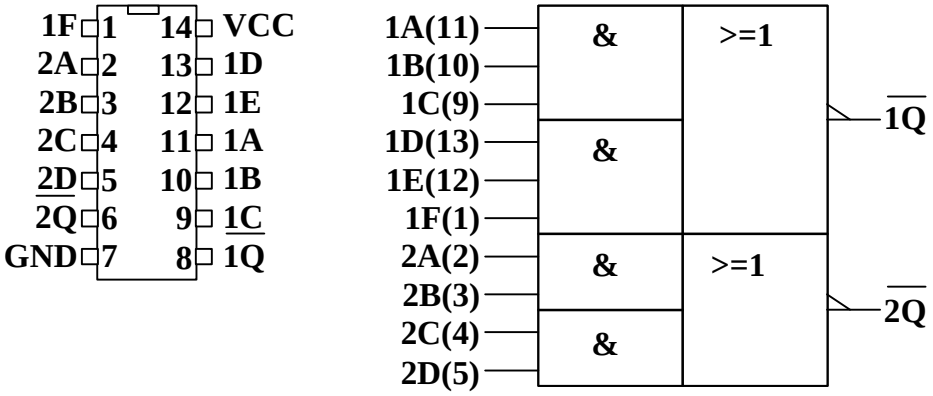
INPUTS						IN/OUT	OUTPUT
D3	D2	D1	D0	LT	RBI	BI/RBO	Q*
X	X	X	X	L	X	H	8
X	X	X	X	X	X	L	-
L	L	L	L	H	L	L	-
L	L	L	L	H	H	H	0
L	L	L	H	H	X	H	1
L	L	H	L	H	X	H	2
.	.	.	.	.	.	.	.
H	H	H	H	H	X	H	15



*)decoded figure, segment outputs H

74x51:

Dual AND/NOR combination gate
Zwei AND/NOR Kombinationsgatter



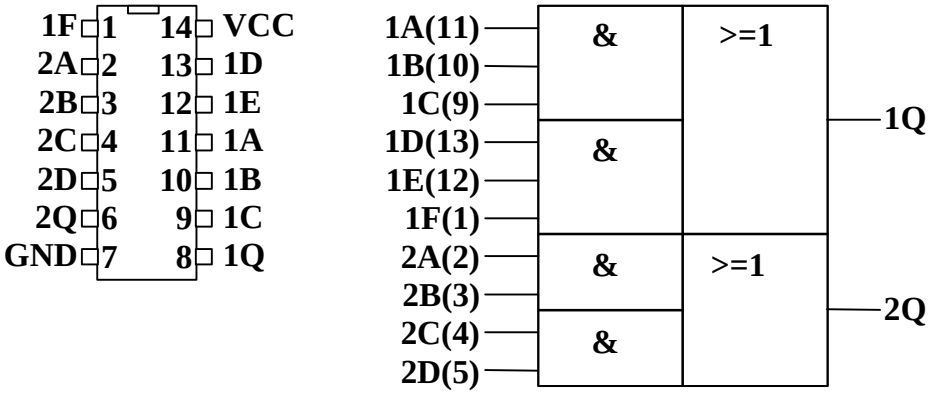
INPUT				OUTPUT
2A	2B	2C	2D	$\overline{2Q}$
H	H	X	X	L
X	X	H	H	L
all other combinations				H

INPUT						OUTPUT
1A	1B	1C	1D	1E	1F	$\overline{1Q}$
H	H	H	X	X	X	L
X	X	X	H	H	H	L
all other combinations						H

Some recommended conditions	7451	74H51	74L51	74LS51	74S51	UNIT
Supply current with all outputs high	8	12,8	0,8	1,6	17,8	mA
Supply current with all outputs low	14	24	1,3	2,8	22	mA
High-level input current	40	50	10	20	50	µA
Low-level input current	-1,6	-2	-0,18	-0,4	-2	mA
High-level output current	-400	-500	-200	-400	-1000	µA
Low-level output current	16	20	3,6	8	20	mA
Output max delay, low to high level	22	11	90	20	5,5	ns
Output max delay, high to low level	15	11	60	20	5,5	ns

74x58:

Dual AND/NOR combination gate
Zwei AND/NOR Kombinationsgatter



INPUT				OUTPUT
2A	2B	2C	2D	2Q
H	H	X	X	H
X	X	H	H	H
all other combinations				L

INPUT						OUTPUT
1A	1B	1C	1D	1E	1F	1Q
H	H	H	X	X	X	H
X	X	X	H	H	H	H
all other combinations						L