1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCHES

The HEF4514B is a 1-of-16 decoder/demultiplexer, having four binary weighted address inputs (A_0 to A_3), a latch enable input (EL), and an active LOW enable input ($\overline{E}$). The 16 outputs (O_0 to O_{15}) are mutually exclusive active HIGH. When EL is HIGH, the selected output is determined by the data on A_n. When EL goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is HIGH. At $\overline{E}$ HIGH, all outputs are LOW. The enable input ($\overline{E}$) does not affect the state of the latch. When the HEF4514B is used as a demultiplexer, $\overline{E}$ is the data input and A_0 to A_3 are the address inputs.

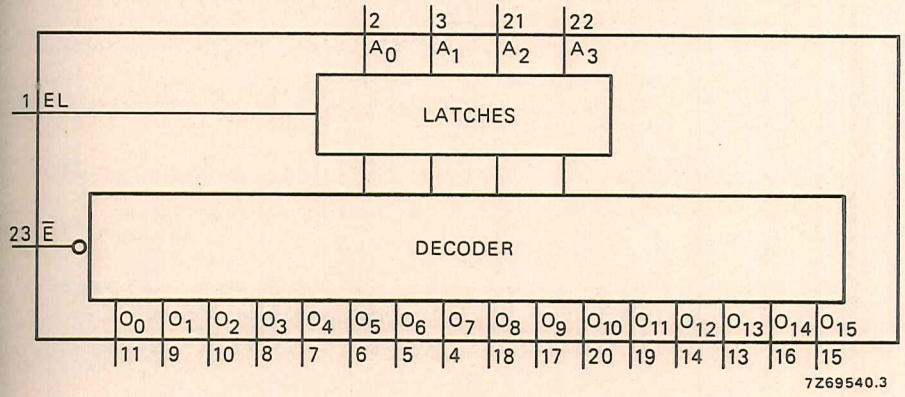

Fig. 1 Functional diagram.

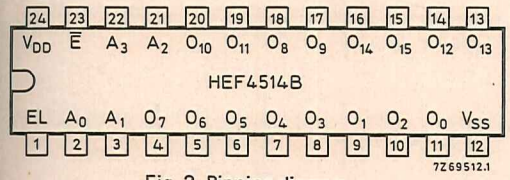

Fig. 2 Pinning diagram.

PINNING

A_0 to A_3	address inputs
$\overline{E}$	enable input (active LOW)
EL	latch enable input
O_0 to O_{15}	outputs (active HIGH)

HEF4514BP: 24-lead DIL; plastic (SOT-101A).
HEF4514BD: 24-lead DIL; ceramic (SOT-94).

APPLICATION INFORMATION

Some examples of applications for the HEF4514B are:

- Digital multiplexing.
- Address decoding.
- Hexadecimal/BCD decoding.

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

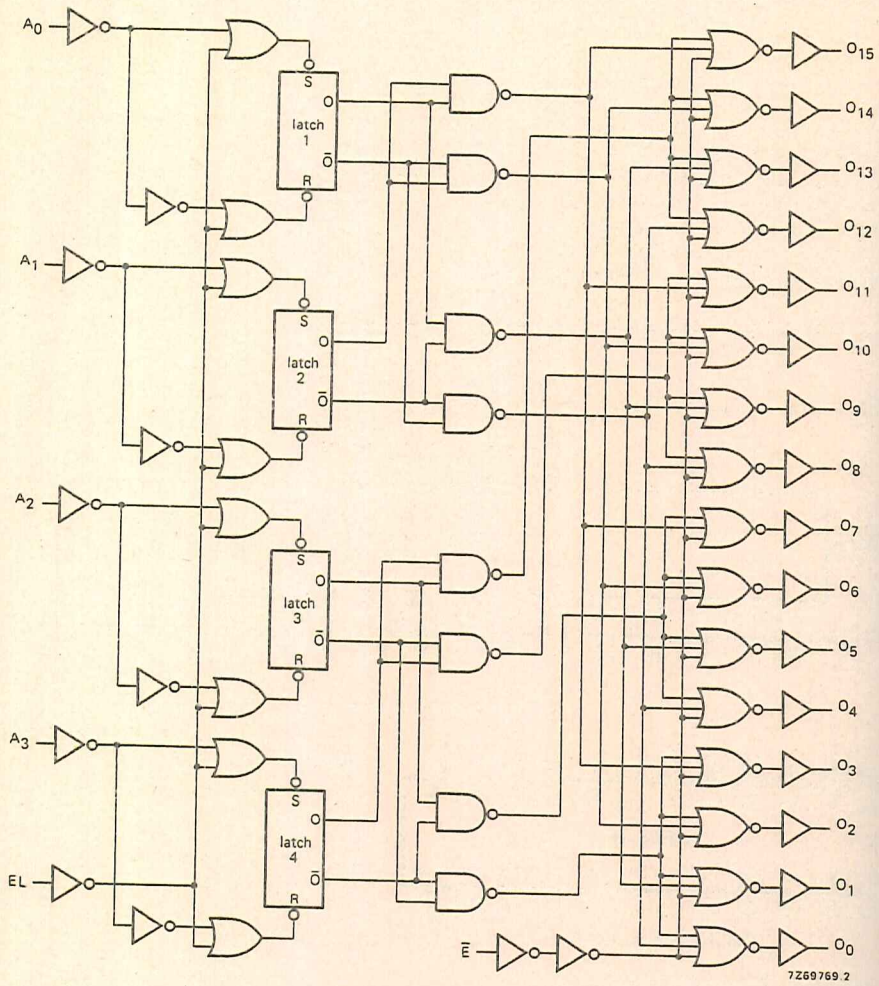

Fig. 3 Logic diagram.

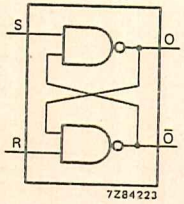

Fig. 4 Logic diagram (one latch).

TRUTH TABLE

inputs					outputs												
$\bar{E}$	A_0	A_1	A_2	A_3	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}	O_{11}	O_{12}	O_{13}	O_{14}	O_{15}
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

EL = HIGH
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
A_n, EL ⟶ O_n	5		260	520	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
	5		270	550	ns	243 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
$\bar{E}$ ⟶ O_n	5		175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	65	130	ns	54 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
	5		200	400	ns	173 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	70	140	ns	59 ns + (0,23 ns/pF) C_L
	15		50	100	ns	42 ns + (0,16 ns/pF) C_L

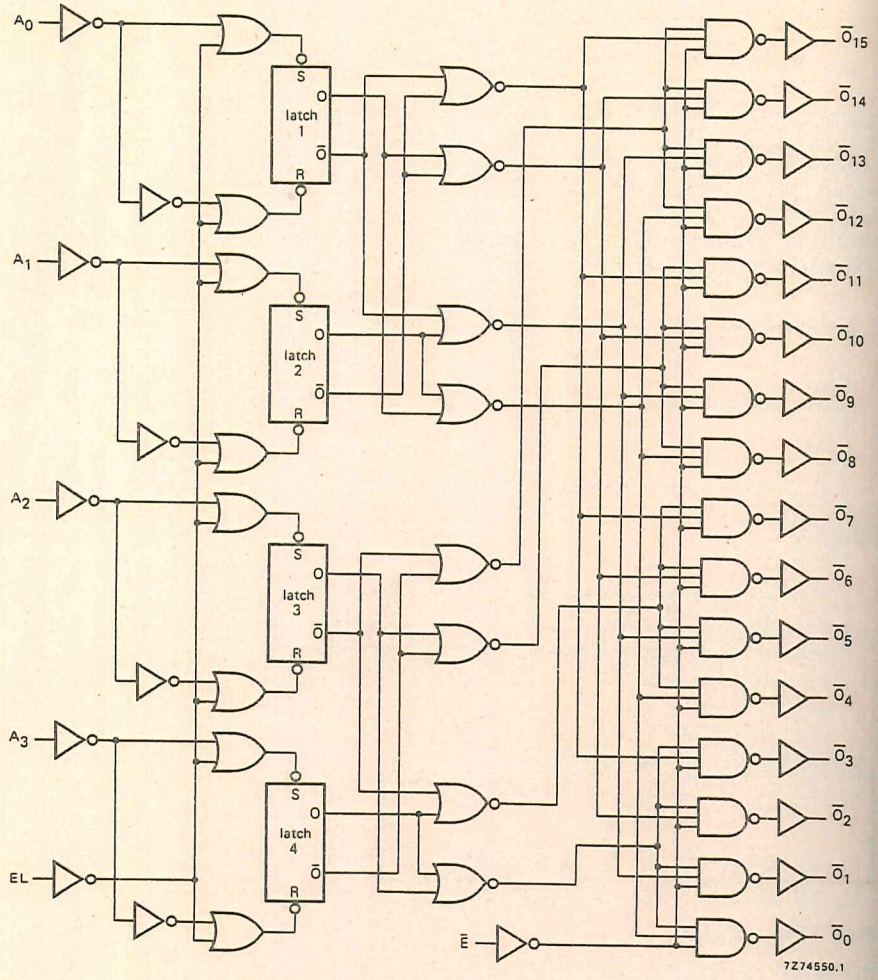

Fig. 3 Logic diagram.

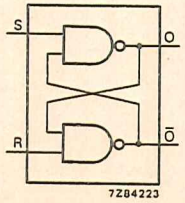

Fig. 4 Logic diagram (one latch).

TRUTH TABLE

inputs					outputs													
$\bar{E}$	A_0	A_1	A_2	A_3	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$	$\bar{O}_8$	$\bar{O}_9$	$\bar{O}_{10}$	$\bar{O}_{11}$	$\bar{O}_{12}$	$\bar{O}_{13}$	$\bar{O}_{14}$	$\bar{O}_{15}$
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

EL = HIGH
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

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Propagation delays						
A_n, EL → $\bar{O}_n$	5		260	520	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
	5		270	550	ns	243 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
$\bar{E}$ → $\bar{O}_n$	5		175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	65	130	ns	54 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
	5		200	400	ns	173 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	70	140	ns	59 ns + (0,23 ns/pF) C_L
	15		50	100	ns	42 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Output transition times	5			90	180 ns	40 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		35	65 ns	14 ns + (0,42 ns/pF) C_L
	15			25	50 ns	11 ns + (0,28 ns/pF) C_L
	5			85	170 ns	35 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		35	70 ns	14 ns + (0,42 ns/pF) C_L
	15			25	50 ns	11 ns + (0,28 ns/pF) C_L
Set-up time	5		120	60	ns	see also waveforms Fig. 5
$A_n \rightarrow$ EL	10	t_{su}	40	20	ns	
	15		30	15	ns	
Hold time	5		0	60	ns	
$A_n \rightarrow$ EL	10	t_{hold}	0	20	ns	
	15		0	15	ns	
Minimum EL pulse width; HIGH	5		120	60	ns	
	10	t_{WELH}	40	20	ns	
	15		30	15	ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1100 f_i + Σ($f_o C_L$) × V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	5500 f_i + Σ($f_o C_L$) × V_{DD}^2	
	15	16 000 f_i + Σ($f_o C_L$) × V_{DD}^2	

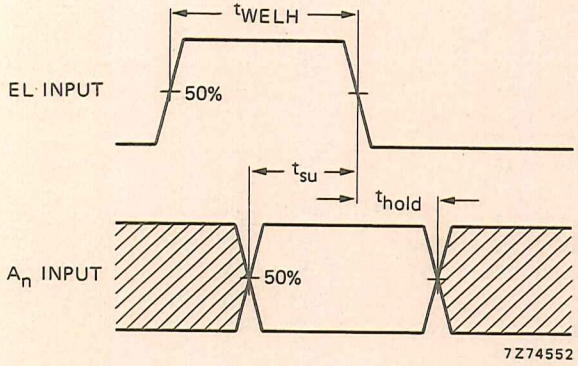

Fig. 5 Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL. Set-up and hold times are shown as positive values but may be specified as negative values.

BINARY UP/DOWN COUNTER

The HEF4516B is an edge-triggered synchronous up/down 4-bit binary counter with a clock input (CP), an up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P_0 to P_3), four parallel outputs (O_0 to O_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR which must be LOW. When PL and $\overline{CE}$ are LOW, the counter changes on the LOW to HIGH transition of CP. Input UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when O_0 to O_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when O_0 to O_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of all other input conditions.

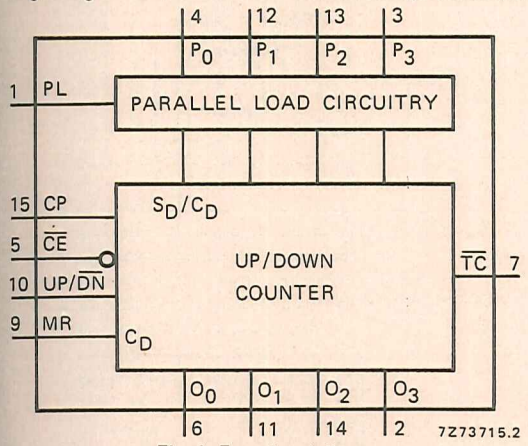

Fig. 1 Functional diagram.

Fig. 2 Pinning diagram.

HEF4516BP: 16-lead DIL; plastic (SOT-38Z).
HEF4516BD: 16-lead DIL; ceramic (SOT-74).
HEF4516BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

PL	parallel load input (active HIGH)	UP/$\overline{DN}$	up/down count control input
P_0 to P_3	parallel inputs	MR	master reset input
$\overline{CE}$	count enable input (active LOW)	$\overline{TC}$	terminal count output (active LOW)
CP	clock pulse input (LOW to HIGH, edge triggered)	O_0 to O_3	parallel outputs

FAMILY DATA, I_{DD} LIMITS category MSI — see Family Specifications